

Capsule Phase Control Thyristor

Consists of a diffused silicon element mounted in an hermetic ceramic cold welded capsule, and features an amplifying gate.
Available in industry standard housing.

| Ratings | Unless otherwise indicated $T_j = 125^\circ\text{C}$ | Maximum Limits | | | | | | | | | Units |
|------------------|--|----------------|-----|-----|-----|------|------|------|------|------|-------|
| | | Voltage Codes | | | | | | | | | |
| | | 02 | 04 | 06 | 08 | 10 | 12 | 14 | 16 | 18 | |
| V_{DRM} | Repetitive peak off-state voltage | 200 | 400 | 600 | 800 | 1000 | 1200 | 1400 | 1600 | 1800 | V |
| V_{DSM} | Non-repetitive peak off-state voltage | 200 | 400 | 600 | 800 | 1000 | 1200 | 1400 | 1600 | 1800 | V |
| V_{RRM} | Repetitive peak reverse voltage | 200 | 400 | 600 | 800 | 1000 | 1200 | 1400 | 1600 | 1800 | V |
| V_{RSM} | Non-repetitive peak reverse voltage | 300 | 500 | 700 | 900 | 1100 | 1300 | 1500 | 1700 | 1900 | V |

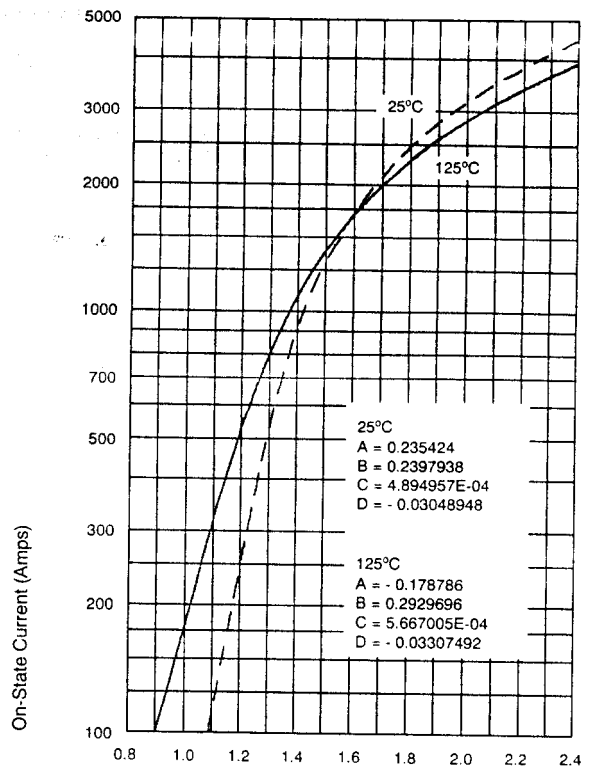
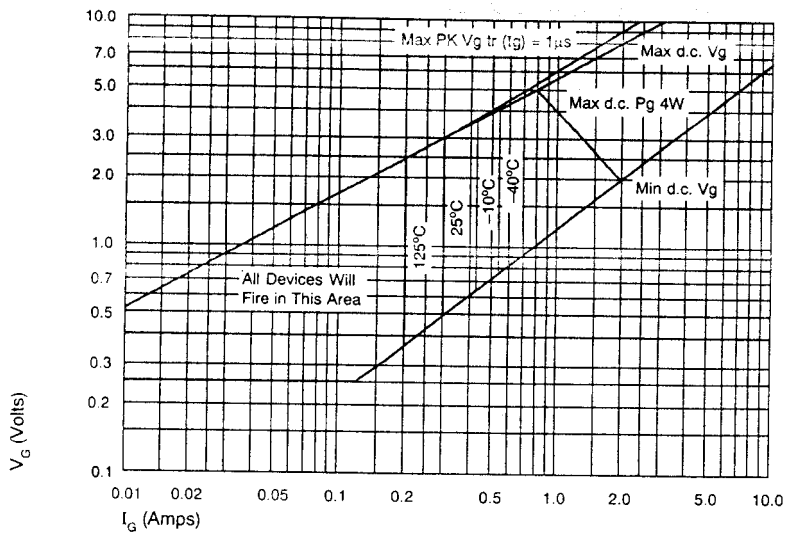
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|---------------------|---|--|--|--|--|--|--|--|--|--|-------------------|----------------------|
| $I_{\text{T(AV)}}$ | Average on-state current | Half sine wave $\left\{ \begin{array}{l} 55^\circ\text{C heatsink temperature} \\ \text{(double side cooled)} \\ 85^\circ\text{C heatsink temperature} \\ \text{(single side cooled)} \end{array} \right.$ | | | | | | | | | 1130 | A |
| $I_{\text{T(RMS)}}$ | R.M.S on-state current | 25°C heatsink temperature, double side cooled | | | | | | | | | 445 | A |
| I_{T} | Continuous on-state current | 25°C heatsink temperature, double side cooled | | | | | | | | | 2260 | A |
| $I_{\text{TSM(1)}}$ | Peak one-cycle surge | 10ms duration, 60% V_{RRM} re-applied | | | | | | | | | 1890 | A |
| $I_{\text{TSM(2)}}$ | Peak one-cycle surge | 10ms duration, $V_{\text{R}} \leq 10$ volts | | | | | | | | | 12700 | A |
| $I^2 t_{(2)}$ | Maximum permissible surge energy | 10ms duration, $V_{\text{R}} \leq 10$ volts | | | | | | | | | 14000 | A |
| I_{FGM} | Peak forward gate current | 3ms duration, $V_{\text{R}} \leq 10$ volts | | | | | | | | | 975×10^3 | A^2s |
| V_{FGM} | Peak forward gate voltage | Anode positive with respect to cathode | | | | | | | | | 720×10^3 | A^2s |
| V_{RGM} | Peak reverse gate voltage | Anode positive with respect to cathode | | | | | | | | | 7.5 | A |
| P_{GM} | Average gate power | | | | | | | | | | 10 | V |
| P_{GM} | Peak gate power | 100µs pulse width | | | | | | | | | 5 | V |
| dv/dt | Rate of rise of off-state voltage | Linear to 80% V_{DRM} gate open-circuit | | | | | | | | | 4 | W |
| $di/dt_{(1)}$ | Rate of rise of on-state current (repetitive) | Gate drive 20 volts, 20 ohms with $t_r \leq 1\mu\text{s}$. | | | | | | | | | 30 | W |
| $di/dt_{(2)}$ | Rate of rise of on-state current (non-repetitive) | Anode voltage $\leq 80\% V_{\text{DRM}}$ | | | | | | | | | *200 | V/µs |
| T_j | Operating temperature range | | | | | | | | | | 500 | A/µs |
| T_{stg} | Storage temperature range | | | | | | | | | | 1000 | A/µs |
| | | | | | | | | | | | -40 to +125 | °C |
| | | | | | | | | | | | -40 to +150 | °C |

| Characteristics | | Unless otherwise indicated $T_j = 125^\circ\text{C}$ | | | | |
|-----------------------|--|--|--|--|-------|-----|
| V_{TM} | Peak on-state voltage | $I_{\text{TM}} = 1700$ A | | | 1.59 | V |
| V_{O} | Forward conduction threshold voltage | | | | 1.06 | V |
| r | Forward conduction slope resistance | | | | 0.312 | mΩ |
| I_{DRM} | Repetitive peak off-state current | At V_{DRM} | | | 60 | mA |
| I_{RRM} | Repetitive peak reverse current | At V_{RRM} | | | 60 | mA |
| I_{GT} | Gate current required to fire all devices | At 25°C, $V_{\text{A}} = 10$ V, $I_{\text{A}} = 2$ A | | | 300 | mA |
| V_{GT} | Gate voltage required to fire all devices | | | | 3.0 | V |
| I_{H} | Holding current | | | | 1.0 | A |
| V_{GO} | Gate voltage which will not trigger any device | | | | 0.25 | V |
| $R_{\text{th(j-hs)}}$ | Thermal resistance, junction to heat sink | Double side cooled | | | 0.032 | K/W |
| | | Single side cooled | | | 0.064 | K/W |

Ordering Information (Please quote device code as explained below)

| N370 | C H | • • | * dv/dt Code for 80% V_{DRM} |
|-----------------|--|-------------------------------|---|
| Fixed Type Code | Outline Code Nominal Thickness CH - 26.2 | Voltage Code (see ratings) | 200V/µs - No Code 300V/µs - GOO 400V/µs - HOO 500V/µs - JOO 750V/µs - KOO 1000V/µs - LOO |

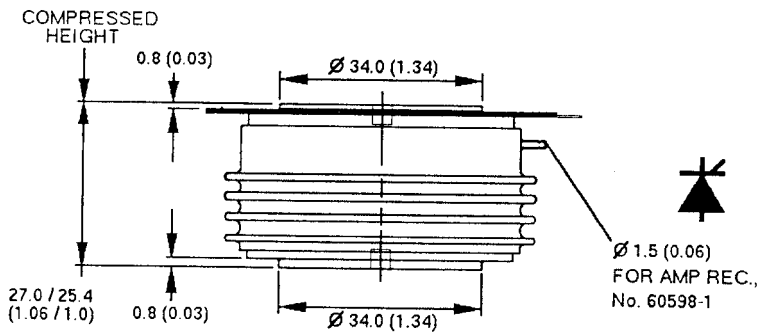
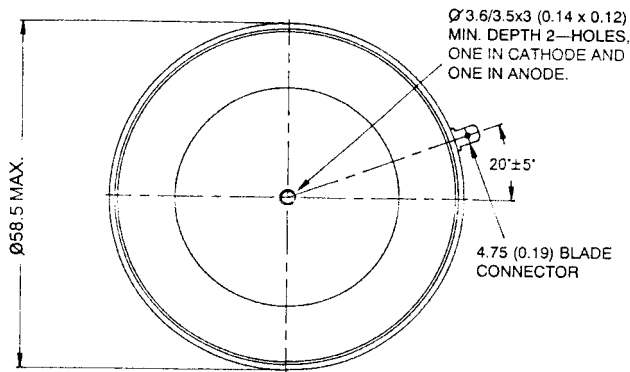
Typical code: N370CH16LOO, 1600 V_{DRM} , 1600 V_{RRM} , 1000V/µs dv/dt to 80% V_{DRM}



On-State Voltage (Volts)

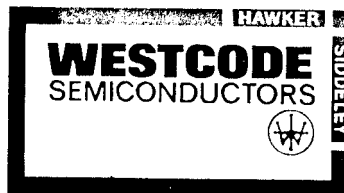
Forward Volt-Drop Calculations:

$$V_T = A + B \ln I_T + C I_T + D \sqrt{I_T}$$



Standard gate leads, 300mm long, available on request.

In the interest of product improvement, Westcode reserves the right to change specifications at any time without notice. © Westcode Semiconductors Ltd.



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